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				Application Number	10/627843
				Filing Date	July 25, 2003
				First Named Inventor	Ge Nong
				Art Unit	4142 2824
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	02-HK-076

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS						
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NON PATENT LITERATURE DOCUMENTS				
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PL	C1	Iyer, et al., "Analysis of a Memory Architecture for Fast Packet Buffers", In Proc. IEEE HPSR, Dallas, Texas, pp. 368-373; 2001, 7803-6711-1/01.		
PL	C2	Mike Clendenin; "IBM shows faster approach to embedded DRAM", EE Times, June 10, 2002. URL: http://www.embedded.com/showArticle.html?articleID=10804520 .		

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Examiner Signature	Pto M. Luu	Date Considered	9/24/04
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